successive sets of output data;

a master controller for setting up the memory system using control commands associated with a set of input data and a set of output data; and

a control unit for, on the basis of the control commands, selecting a first memory circuit and generating a write-address for the first memory circuit when a data from the set of input data is provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address in the second memory circuit when a data from the set of output data is required by the second processor.

2. (As Amended) A data processing arrangement, as claimed in claim 1, wherein the control unit comprises:

a write-counter whose value is modified in association with the data received from the set of input data and which value indicates the write-address of the data in the first memory circuit; and

a read-counter whose value is modified in association with the data provided from the set of output data and which value indicates the read-address of the data in the second memory circuit.

3. (As Amended) A data processing arrangement, as claimed in claim 1, wherein the control unit comprises a write-input port for receiving a write-data signal from the first processor in response

to which the control unit generates the write-address and the control unit further comprises a read-input port for receiving a read-data signal from the second processor in response to which the control unit generates the read-address.

4. (As Amended) A memory system comprising:

a plurality of memory circuits for receiving successive sets of input data and for providing successive sets of output data;

a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a write-address for the first memory circuit, when a data from the set of input data is received, and for selecting a second memory circuit and generating a read-address for the second memory circuit, when a data from the set of output data is provided.

5. (As Amended) A method of processing data in a data processing arrangement including a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system including a plurality of memory circuits for receiving the successive sets of input data and providing the successive sets of output data,

the method comprising, for a set of input data and a set of output data, the following steps: